1. A method for fabricating IC's comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask, two hard mask layers, over the intermetal dielectric layer;

(e) patterning the intermetal dielectric layer and hard mask layers, and etching to form via openings;

(f) coating with a photoresist material, forming a bottom anti-reflective coating over the top intermetal dielectric layer and filling the via opening;

(g) patterning the intermetal dielectric layer and hard mask layers, and etching to form trench openings;

(h) stripping-off all photoresist material, thus forming open trench and open via regions for subsequent conducting metal fill.

2. The method of claim 1, wherein said substrate is semiconductor single crystal silicon or an IC module.

3. The method of claim 1, wherein said conducting material is selected from following group comprised of: metal wiring or contacts of Cu, AlCu alloys, AlCuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

4. The method of claim 1, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide and undoped silicate glass.

5. The method of claim 1, wherein said bi-layered hard mask is comprised of:

HM1/ HM2/ IMD stack, inter-metal dielectric

<u>HM1</u> <u>HM2</u> <u>IMD</u>

USG/ SiC or SiN/ Fluorine doped Oxide or SiO_2

USG/ SiC / Carbon-doped Oxide

USG/ SiC / Organic based low-k dielectric

USG/ SiC / porous low-k dielectric

where USG, undoped silicate glass for HM1 layer, hard mask top layer, also can be a conventional SiO_2 film of thickness in the range from 1000 to 2000 Angstroms, and HM2, hard mask bottom layer, is a selective dielectric layer (Selectivity of ~3-5) for HM1 etch, with etch stop on HM2, the HM2 is between approximately 300 to 600 Angstroms thick, the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

6. The method of claim 1, wherein said photoresist material forming a bottom anti-reflective coating is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

7. The method of claim 1, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching BARC opening,
Step 2: CF_4 / CF_3 / Ar based for HM1 etch,
Step 3: N_2 / O_2 based for etching via-fill material recess,
Step 4: CF_4 / N_2 / O_2 based for HM2 and IMD etch,
Step 5: O_2 based for Ashing, and
Step 6: CF_3 / N_2 based for bottom etch stop layer etch.

8. The method of claim 1, wherein multilevel structures are fabricating by repeating steps (b) through (h), described above.

9. A method of fabricating an integrated circuit with a dual damascene process using a bi-layer hard mask, the method comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask, two hard mask layers, over the intermetal dielectric layer;

(e) patterning the intermetal dielectric layer and hard mask layers, and etching to form via openings;

(f) coating with a photoresist material, forming a bottom anti-reflective coating over the top intermetal dielectric layer and filling the via opening;

(g) patterning the intermetal dielectric layer and hard mask layers, and etching to form trench openings;

(h) stripping-off all photoresist material, forming open trench and open via regions;

(i) depositing a copper seed layer in the trench openings and via openings;

(j) forming an excess of copper metal over the copper seed layer;

(k) planarizing the excess copper back, thus forming inlaid copper in the trench and via openings for contact vias and interconnect wiring.

10. The method of claim 9, wherein said substrate is semiconductor single crystal silicon or an IC module.

11. The method of claim 9, wherein said conducting material is selected from following group comprised of: metal wiring or contacts of Cu, AlCu alloys, AlCuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

12. The method of claim 9, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide and undoped silicate glass.

13. The method of claim 9, wherein said bi-layered hard mask is comprised of:

HM1/ HM2/ IMD stack, inter-metal dielectric

HM1	HM2	IMD
USG/	SiC or SiN/	Fluorine doped Oxide or SiO_2
USG/	SiC /	Carbon-doped Oxide
USG/	SiC /	Organic based low-k dielectric
USG/	SiC /	porous low-k dielectric

where USG, undoped silicate glass for HM1 layer, hard mask top layer, also can be a conventional SiO_2 film of thickness in the range from 1000 to 2000 Angstroms, and HM2, hard mask bottom layer, is a selective dielectric layer (Selectivity of ~3-5) for HM1 etch, with etch stop on HM2, the HM2 is between approximately 300 to 600 Angstroms thick, the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

14. The method of claim 9, wherein said photoresist material forming a bottom anti-reflective coating is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

15. The method of claim 9, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching BARC opening,

Step 2: CF_4 / CF_3 / Ar based for HM1 etch,

Step 3: N_2 / O_2 based for etching via-fill material recess,

Step 4: CF_4 / N_2 / O_2 based for HM2 and IMD etch,

Step 5: O_2 based for Ashing, and

Step 6: CF_3 / N_2 based for bottom etch stop layer etch.

16. The method of claim 9, further comprising depositing and defining a copper seed layer, in the via and trench openings, comprised of copper, with thickness maximum of approximately 3,000 Angstroms.

17. The method of claim 9, further comprising depositing a conducting metal fill of electrochemically deposited copper upon a copper seed layer, in the via and trench openings, with thickness maximum of approximately 20,000 Angstroms, forming an excess of copper over the vias and trenches.

18. The method of claim 9, further comprising planarizing an excess of copper over the vias and trenches by chemical mechanical polish, milling, ion milling, and/or etching, forming inlaid dual damascene conducting metal interconnects and contact vias in the vias and trenches.

19. The method of claim 9, wherein multilevel structures are fabricating by repeating steps (b) through (k), described above.

20. A method of fabricating an integrated circuit with a dual damascene process for applications in MOSFET CMOS memory and logic devices, using a bi-layer hard mask, the method comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask, two hard mask layers, over the intermetal dielectric layer;

(e) patterning the intermetal dielectric layer and hard mask layers, and etching to form via openings;

(f) coating with a photoresist material, forming a bottom anti-reflective coating over the top intermetal dielectric layer and filling the via opening;

(g) patterning the intermetal dielectric layer and hard mask layers, and etching to form trench openings;

(h) stripping-off all photoresist material, forming open trench and open via regions;

(i) depositing a copper seed layer in the trench openings and via openings;

(j) forming an excess of copper metal over the copper seed layer;

(k) planarizing the excess copper back, thus forming inlaid copper in the trench and via openings for contact vias and interconnect wiring.

21. The method of claim 20, wherein said substrate is semiconductor single crystal silicon or an IC module.

22. The method of claim 20, wherein said conducting material is selected from following group comprised of: metal wiring or contacts of Cu, AlCu alloys, AlCuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

23. The method of claim 20, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide and undoped silicate glass.

24. The method of claim 20, wherein said bi-layered hard mask is comprised of:

HM1/ HM2/ IMD stack, inter-metal dielectric

HM1	HM2	IMD
USG/	SiC or SiN/	Fluorine doped Oxide or SiO_2
USG/	SiC /	Carbon-doped Oxide
USG/	SiC /	Organic based low-k dielectric
USG/	SiC /	porous low-k dielectric

where USG, undoped silicate glass for HM1 layer, hard mask top layer, also can be a conventional SiO_2 film of thickness in the range from 1000 to 2000 Angstroms, and HM2, hard mask bottom layer, is a selective dielectric layer (Selectivity of ~3-5) for HM1 etch, with etch stop on HM2, the HM2 is between approximately 300 to 600 Angstroms thick, the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

25. The method of claim 20, wherein said photoresist material forming a bottom anti-reflective material is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

26. The method of claim 20, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching BARC opening,

Step 2: CF_4 / CF_3 / Ar based for HM1 etch,

Step 3: N_2 / O_2 based for etching via-fill material recess,

Step 4: CF_4 / N_2 / O_2 based for HM2 and IMD etch,

Step 5: O_2 based for Ashing, and

Step 6: CF_3 / N_2 based for bottom etch stop layer etch.

27. The method of claim 20, further comprising depositing and defining a copper seed layer, in the via and trench openings, comprised of copper, with thickness maximum of approximately 3,000 Angstroms.

28. The method of claim 20, further comprising depositing a conducting metal fill of electrochemically deposited copper upon a copper seed layer, in the via and trench openings, with thickness maximum of approximately 20,000 Angstroms, forming an excess of copper over the vias and trenches.

29. The method of claim 20, further comprising planarizing an excess of copper over the vias and trenches by chemical mechanical polish, milling, ion milling, and/or etching, forming inlaid dual damascene conducting metal interconnects and contact vias in the vias and trenches.

30. The method of claim 20, wherein multilevel structures are fabricating by repeating steps (b) through (k), described above.

31. A bi-layered hard mask structure comprising:

HM1/ HM2/ IMD stack, inter-metal dielectric

<u>HM1</u> <u>HM2</u> <u>IMD</u>

USG/ SiC or SiN/ Fluorine doped Oxide or SiO_2

USG/ SiC / Carbon-doped Oxide

USG/ SiC / Organic based low-k dielectric

USG/ SiC / porous low-k dielectric

where USG, undoped silicate glass for HM1 layer, hard mask top layer, also can be a conventional SiO_2 film of thickness in the range from 1000 to 2000 Angstroms, and HM2, hard mask bottom layer, is a selective dielectric layer (Selectivity of ~3-5) for HM1 etch, with etch stop on HM2, the HM2 is between approximately 300 to 600 Angstroms thick, the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

32. The bi-layered hard mask structure of claim 31 wherein the first layer is USG, undoped silicate glass, thickness ranges from 1,000 to 2,000 Angstroms, and the second layer is comprised of SiC or SiN, with thickness ranges from 300 to 600 Angstroms, over the inter-metal dielectric, with thickness maximum of 20,000 Angstroms.